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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/085,929	02/28/2002	Keith W. Holt	01-975	4364	
24319 7	590 11/03/2004		EXAM	EXAMINER	
LSI LOGIC C	CORPORATION		LAMARR	E, GUY J	
MS: D-106	CEILLE		ART UNIT	PAPER NUMBER	
MILPITAS, C	A 95035		2133		

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



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		Application No.	Applicant(s)	/			
		10/085,929	HOLT, KEITH W.	- (
	Office Action Summary	Examiner	Art Unit	-			
		Guy J. Lamarre, P.E.	2133				
Period fo	The MAILING DATE of this communication	n appears on the cover sheet wit	h the correspondence address -	-			
THE - Extended after - If the - If NO - Failu - Any	ORTENED STATUTORY PERIOD FOR R MAILING DATE OF THIS COMMUNICATI missions of time may be available under the provision of 37 C 5K (p) MONTH's from the making date of this communicati period for perly period above is less than thirty (30) days, period for reply as specified above, the maximum statutory in period for reply as specified above, the maximum statutory in period for reply service by the Office ident than three months, after this dd patent term edjustment. See 37 GFR 1704(b).	ION. FR 1.136(a). In no event, however, may a reon, a reply within the statutory minimum of thirty period will expire SIX (6) MON1 statute, cause the application to become AB	ply be timely filed (30) days will be considered timely. FHS from the mailing date of this communicated the communicated the state of this communicated the state of	ation.			
1)🛛	Responsive to communication(s) filed on	28 February 2002.					
		This action is non-final.					
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
4)⊠	Claim(s) <u>1-18</u> is/are pending in the application 4a) Of the above claim(s) is/are with						
5)□	Claim(s) is/are allowed.						
6)🖂	☑ Claim(s) <u>1-18</u> is/are rejected.						
	Claim(s) is/are objected to.						
8)	Claim(s) are subject to restriction a	and/or election requirement.					
Applicat	ion Papers						
	The specification is objected to by the Exa						
10)⊠	The drawing(s) filed on 2/28/02 is/are: a)		-				
	Applicant may not request that any objection to		* *				
44)□	Replacement drawing sheet(s) including the co						
	The oath or declaration is objected to by the	he Examiner. Note the attached	Office Action or form PTO-152	<u>?</u> .			
-	under 35 U.S.C. §§ 119 and 120						
	Acknowledgment is made of a claim for fo All b) Some * c) None of: 1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International B	ments have been received. ments have been received in Appriority documents have been	oplication No				
13)□ A s 3 a	See the attached detailed Office action for a Acknowledgment is made of a claim for dor ince a specific reference was included in the 7 CFR 1.78. b) The translation of the foreign language	a list of the certified copies not a mestic priority under 35 U.S.C. the first sentence of the specifical re provisional application has be	§ 119(e) (to a provisional application or in an Application Data Seen received.	Sheet.			
	Acknowledgment is made of a claim for dor eference was included in the first sentence						
Attachmen	* *						
2) Notice	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-94) mation Disclosure Statement(s) (PTO-1449) Paper N	5) 5) Notice of In	ummary (PTO-413) Paper No(s) formal Patent Application (PTO-152)				
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DETAILED ACTION

Pursuant to 35 USC 131, Claims 1-18 are presented for examination.

Specification

2. The disclosure is objected to because para. 6 recites: 'an all' instead of 'on all,' and algorithm 300 as described in para 23 is not seen in the referred figure. Specification to be amended accordingly. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.1 Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwatani (US Patent No. 6,023,780).

Iwatani anticipates the claimed invention because disclosed is means to access data for detecting drive errors wherein plural drives are congregated into a single disk configuration with means to generate metadata, means to distribute along with data address/location tagging means via temporal/spatial coordinate means to keep track such data and metadata through plural RAID levels, and means to compare such data and metadata to determine and correct disk anomalies.

Iwatani teaches, in Figs. 1-17 and related description, a disc array apparatus which 'comprises a section generating, when data is stored in the data memory device and first redundancy information is stored in the first redundancy information memory device, relevant data including second redundancy information corresponding to the first redundancy information and to be stored in the second redundancy information memory device. The disc array apparatus of the present invention further comprises a section judging, when the data is read from the plurality of data memory devices, the normality of the data on the basis of the second redundancy information stored in the second redundancy information memory device. In addition, the disc array apparatus of

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the present invention also comprises a restructuring section designating, when the data is judged to be abnormal, only one memory device among a plurality of memory devices as storing the abnormal data, and restructuring (recovering) the data stored in the designated memory device on the basis of the information stored in the remaining memory devices other than the designated memory device.'

As per claim 1, Iwatani discloses the claimed method for detecting drive anomalies in col. 2 lines 25-44, comprising: (a) verifying data is written to a media upon an occurrence of a write operation in col. 1 lines 50-54; (b) performing a data block integrity test by reading data from a single drive (in col. 1 line 55) during an occurrence of a read operation in col. 1 line 55; and (c) performing a location check by reading data from said single drive (in col. 1 lines 63-67) during said occurrence of said read operation in col. 4 line 66, wherein a data persistency verification is not performed during said read operation in col. 2 lines 1-6, 38-44, 67. As per claim 2, Iwatani discloses the claimed method as claimed in claim 1, wherein said data persistency verification determines whether data is written to said media in col. 2 line 63. As per claim 3, Iwatani discloses the claimed method as claimed in claim 1, wherein a random read performance is increased by removing the requirement of reading a form of metadata from a second drive in col. 2 line 63 - col. 3 line 3 wherein data is mirrored to thereby avoid the need for reading metadata 2nd such parity information for drive. As per claim 4, Iwatani discloses the claimed method as claimed in claim 1, wherein said data block integrity test ensures that data has been retrieved properly in col. 3 lines 54-65 and Fig. 3: S68.

As per claim 5, Iwatani discloses the claimed method as claimed in claim 1, wherein said location check ensures that data has been retrieved from a correct physical location in col. 3 lines 54-65.

As per claim 6, Iwatani discloses the claimed method for detecting drive anomalies in col. 2.

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lines 25-44, comprising: (a) verifying data is written to a media upon an occurrence of a write operation in col. 1 lines 50-54; (b) performing a data block integrity test by reading data from a single drive (in col. 1 line 55) during an occurrence of a read operation in col. 1 line 55; said data block integrity test employing a parity error detection algorithm (in col. 10 lines 48-67 wherein parity/CRC comparing means is provided plural data/metadata for matching/discriminating operations);; and (c) performing a location check by reading data from said single drive during said occurrence of said read operation, said location check including the comparison of a location tag with an expected value, wherein a data persistency verification is not performed during said read operation in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location tag means to ensure that data access is properly implemented.

As per claim 7, Iwatani discloses the claimed method as claimed in claim 6, wherein said data persistency verification determines whether data is written to said media in col. 2 line 63.

As per claim 8, Iwatani discloses the claimed method as claimed in claim 6, wherein a random read performance is increased by removing the requirement of reading a form of metadata from a second drive in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location tag means to ensure that data access is properly implemented.

As per claim 9, Iwatani discloses the claimed method as claimed in claim 6, wherein said data block integrity test ensures that data has been retrieved properly in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location tag means to ensure that data access is properly implemented.

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As per claim 10, Iwatani discloses the claimed method as claimed in claim 6, wherein said location check ensures that data has been retrieved from a correct physical location in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location tag means to ensure that data properly implemented. access As per claim 11, Iwatani discloses the claimed method as claimed in claim 6, wherein said parity error detection algorithm is a cyclic redundancy check in col. 10 lines 48-67 wherein parity/CRC comparing means is provided for plural data/metadata matching/discriminating operations.

As per claim 12, Iwatani discloses the claimed method of detecting drive anomalies during a read operation, comprising: (a) reading data from a single drive (in col. 1 line 55) into a cache memory (in col. 13 lines 35-59 wherein storing means is provided for plural distinct data transfer operation in the disk controller); (b) generating a first parity error information set for a data read from said drive in col. 10 lines 48-67; (c) comparing a second parity error information set with said first parity error information set (in col. 10 lines 48-67 wherein parity/CRC comparing means is provided for plural data/metadata matching/discriminating operations); and (d) comparing a location tag with an expected value (in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location tag means), wherein a data integrity test and location check is performed by reading data from said single drive(in col. 1 line 55). As per claim 13, Iwatani discloses the claimed method as claimed in claim 12, wherein data has been retrieved correctly from said single drive when said first parity error information set matches said second parity information lines 48-67 As per claim 14, Iwatani discloses the claimed method as claimed in claim 13, wherein said

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second parity error information set is stored as metadata in col. 10 lines 48-67. As per claim 15, Iwatani discloses the claimed method as claimed in claim 13, wherein said first parity error information set and said second parity error information set are cyclic redundancy check information in col. 10 lines 48-67 As per claim 16, Iwatani discloses the claimed method as claimed in claim 12, wherein data has been retrieved from a correct physical location when said location tag matches said expected value in col. 10 lines 48-67 wherein data striping means, e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in predetermined address/location range via location means. As per claim 17, Iwatani discloses the claimed method as claimed in claim 16, wherein said location tag provides an indication of an address range associated with a data block in col. 10 lines 48-67 wherein data striping means e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in address/location range via location tag means. As per claim 18, Iwatani discloses the claimed method as claimed in claim 17, wherein a range of said address range is flexible in col. 10 lines 48-67 wherein data striping means e.g., RAID 2, is provided for partitioning data and parity as metadata and storing same in flexible address range.

Conclusion

- The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 4.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to: (703) 872-9306 for all formal communications. Application/Control Number: 10/085,929

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Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Guy J. Lamarre, P.E Primary Examiner 10/28/04